A STUDY OF TRANSISTORS CONNECTED IN PARALLEL*

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ABSTRACT. An analysis has been carried out of the problem of an amplifier using two transistors in parallel. It has been shown that the performance of the combination may be conveniently studied in terms of a single equivalent transistor whose parameters are related to those of the individual transistors in a simple manner. Expressions have been deduced for the gain and the input and the output impedances of the parallel combination for all the three basic modes of operation *viz.*, grounded base and grounded emitter and grounded collector connection. Results of experiments both for point contact and for junction transistors are found to be in good agreement with the results of the theoretical analysis.

1. INTRODUCTION

One of the main drawbacks of transistors as a substitute for vacuum tube amplifier is the small amount of power it can handle. This drawback may be overcome to some extent by using two transistors in pushpull or in parallel arrangement. The former may be used where efficiency of operation is an important consideration and the latter when this is not so. Pushpull operation, involving the use of transformers, however, enhances the cost and reduces the compactness of the equipment. To obviate this, one may use a transistor of p-n-p type in conjunction with another of n-p-n type. But this makes the power supply system complicated. A reasonable efficiency combined with large power handling capacity may be achieved with transistors connected in parallel, and study of the performance of transistors so arranged is thus of practical importance. This study has been made for both point contact and junction transistors and an account of the results obtained is presented in the paper. In section 2 is given a general analysis of the problem of a grounded base amplifier using two transistors in parallel and in section 3, a method by which the various working formulae for such an amplifier may be obtained by reducing the combination to a single equivalent transistor. This is followed in section 4 by results of experiments which support the theoretical deductions as given in section 3.

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2. ANALYSIS OF GROUNDED BASE AMPLIFIER USING TWO TRANSISTORS IN PARALLEL

The equivalent circuit of a single point contact or junction transistor amplifier for grounded base operation is shown in figure 1. The symbols r_e, r_b & r_c denote respectively the emitter, base and collector resistances and $i_e r_m$ the active element introduced to take into account the current gain of the transistor. i_e and i_c represent the emitter and collector currents respectively and R_S and R_L denote the source and load resistances respectively.

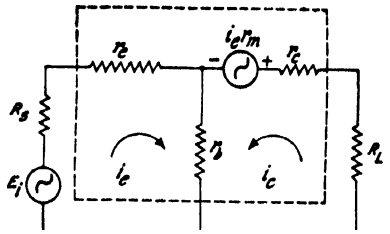

Fig. 1 : Showing the equivalent circuit of a grounded base transistor amplifier.

It follows from figure 1 that for the case of a grounded base amplifier using two transistors in parallel, the equivalent circuit would take the form as shown in figure 2. The various resistances and currents of the second transistor are denoted by primed symbols in order to emphasize that the two transistors may not always be of identical characteristics.

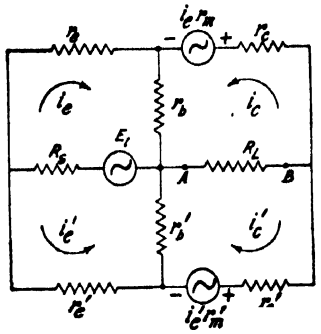

Fig. 2 : Showing the equivalent circuit of a grounded base amplifier using two transistors in parallel.

Applying Kirchoff's laws to the 4 meshes of figure 2, the following equations are obtained :

$$\left.\begin{aligned}
(r_e + r_b + R_S).i_e + r_b.i_c + R_S.i'_e + 0.i'_c &= E_i \\
R_S.i_e + 0.i_c + (r'_e + r'_b + R_S)i'_e + r'_b.i'_c &= E_i \\
(r_b + r_m)i_e + (r_b + r_c + R_L)i_c + 0.i'_e + R_L.i'_e &= 0 \\
0.i_e + R_L.i_c + (r'_b + r'_m).i'_e + (r'_b + r'_{e_c} + R_L)i'_c &= 0
\end{aligned}\right\} \quad (1)$$

These equations may be solved by standard methods. When this is done, i_e, i'_e, i_c and i'_c are found out to be given by:

$$\left.\begin{aligned} i_e &= E_i[-r'_{11}\{(r_{22}+R_L)(r'_{22}+R_L)-R_L^2\}+r'_{21}\{r_{12}R_L+r'_{12}(r_{22}+R_L)\}]/\Delta_p \\ i'_e &= E_i[-r_{11}\{(r_{22}+R_L)(r'_{22}+R_L)-R_L^2\}+r_{21}\{r_{12}(r'_{22}+R_L)+r'_{12}.R_L\}]/\Delta_p \\ i_c &= E_i[-R_L r_{11}r'_{21}+r_{21}\{r'_{11}(r'_{22}+R_L)-r'_{12}r'_{21}\}]/\Delta_p \\ i'_c &= E_i[-R_L r'_{11}r_{21}+r'_{21}\{r_{11}(r_{22}+R_L)-r_{12}r_{21}\}]/\Delta_p \end{aligned}\right\} \quad \ldots (2)$$

where Δ_p = the circuit determinant

$$= -[(r_{11}r_{22}-r_{12}r_{21})(r'_{11}r'_{22}-r'_{12}r'_{21})+R_L\{r_{11}(r'_{11}r'_{22}-r'_{12}r'_{21}) + r'_{11}(r_{11}r_{22}-r_{12}r_{21})\}] \quad \ldots (2a)$$

and r_{11}, r_{22}, r_{12}, r_{21}, r'_{11}, r'_{12} etc. are the open circuit parameters of the transistors defined by:

$$\left.\begin{aligned} r_{11} &= r_e+r_b, \quad r_{12} = r_b; & r'_{11} &= r'_e+r'_b, \quad r'_{12} = r'_b \\ r_{21} &= r_b+r_m, \quad r_{22} = r_b+r_c; & r'_{21} &= r'_b+r'_m, \quad r'_{22} = r'_b+r'_c \end{aligned}\right\} \quad \ldots (2b)$$

It is to be noted that the above solutions are obtained through the assumption that R_S is negligible—a condition which is always satisfied by a practical transistor amplifier circuit.

From (2), we readily get,
in put impedance

$$Z_{in} = \frac{E_i}{i_e+i'_e} = \frac{\Delta\Delta'+R_L(r_{11}\Delta'+r'_{11}\Delta)}{r_{22}\Delta'+r'_{22}\Delta+R_L\{(r_{11}+r'_{11})(r_{22}+r'_{22})-(r_{12}+r'_{12})(r_{21}+r'_{21})\}} \quad (3)$$

where $\Delta = r_{11}r_{22}-r_{12}r_{21}$ and $\Delta' = r'_{11}r'_{22}-r'_{12}r'_{21}$

The output impedance Z_{out} is given by the ratio of the voltage across the points A and B in figure 2, to the sum i_c+i_c' with the generator E_i short-circuited. An analysis in exactly the same manner as carried out above gives

$$Z_{out} = \frac{\Delta\Delta'}{r_{11}\Delta'+r'_{11}\Delta} \quad \ldots (4)$$

The forward power gain ϕ is now readily obtained as

$$\phi = \frac{(i_c+i'_c)^2R_L}{(i_e+i'_e)^2Z_{in}} = Z_{in}.R_L.\left[\frac{r_{21}\Delta'+r_{21}'\Delta}{\Delta\Delta'+R_L(r_{11}\Delta'+r'_{11}\Delta)}\right]^2 \quad \ldots (5)$$

3. THE EQUIVALENT TRANSISTOR

Expressions for input and output impedances and gain of two transistors in parallel as deduced in the previous section may be easily obtained from the known

equations for a single transistor by deriving a single hypothetical transistor whose parameters are equivalent to those of the combination . Parameters of this equivalent transistor may be found out by applying elementary matrix consideration to the circuit shown in figure 2.

The 4-pole equations of a single transistor, taking $R_L = 0$, are

$$\begin{aligned} E_i &= i_e.r_{11}+i_c.r_{12} \\ 0 &= i_e.r_{21}+i_c.r_{22} \end{aligned} \qquad \ldots \quad (6)$$

Hence the impedance matrix is given by

$$|Z| = \qquad \ldots \quad (7)$$

from which by inverse operations, the admittance matrix is obtained as

$$|Y| = \qquad (8)$$

where $\Delta = r_{11}r_{22} - r_{12}r_{21}$

Equation (8) suggests that when two transistors are connected in parallel, the admittance matrix of the combination would be

$$Y_0] = \qquad \ldots \quad (9)$$

where the primed elements refer to the second transistor. By inverse operations, the impedance matrix corresponding to $[Y_0]$ is found out, which after a little simplification is given by:

$$[Z_0] = \qquad \ldots \quad (10)$$

where $P = (r_{11}+r'_{11})(r_{22}+r'_{22}) - (r_{12}+r'_{12})(r_{21}+r'_{21})$ ... (10a)

If now for the equivalent transistor, R_{11}, R_{12}, R_{21} and R_{22} denote the open circuit parameters given by

$$R_{11} = R_e + R_b, \quad R_{12} = R_b,$$
$$R_{21} = R_b + R_m, \quad R_{22} = R_b + R_c,$$

where R_b, R_c, R_e and R_m are the equivalent circuit element values, its impedance matrix would be given by the expression

$$[Z_{eq}] = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} \tag{11}$$

Comparing equations (10) and (11), we obtain

$$\left.\begin{aligned} R_{11} &= \frac{r_{11}\Delta' + r'_{11}\Delta}{P}; \qquad R_{12} = \frac{r_{12}\Delta' + r'_{12}\Delta}{P} \\ R_{21} &= \frac{r_{21}\Delta' + r_{21}'\Delta}{P} \qquad R_{22} \quad \frac{r_{22}\Delta' + r_{22}'\Delta}{P} \end{aligned}\right\} \tag{12}$$

from which the circuit element values are obtained as

$$\left.\begin{aligned} R_e &= \frac{r_e\Delta' + r_e'\Delta}{P}; \qquad R_b = \frac{r_b\Delta' + r_b'\Delta}{P} \\ R_c &= \frac{r_c\Delta' + r_c'\Delta}{P}. \qquad R_m \quad \frac{r_m\Delta' + r_m'\Delta}{P} \end{aligned}\right\} \tag{13}$$

To find out expressions for the input and output impedances and gain for the three modes of operation viz. grounded base, grounded emitter and grounded collector, a method suggested by Shekel (1952) is very helpful.

In this method, the impedance matrix $[Z_{eq}]$ as given in (11) is first converted to its admittance matrix $[Y_{eq}]$ given by

$$[Y_{eq}] = \begin{bmatrix} R_{22}/\Delta_0 & -R_{12}/\Delta_0 \\ -R_{21}/\Delta_0 & R_{11}/\Delta_0 \end{bmatrix} \tag{14}$$

where $$\Delta_0 = R_{11}R_{22} - R_{12}R_{21}$$

A matrix $[Y^0]$ called the "indefinite admittance matrix" is then formed such that the sum of the elements in any row or column is zero. Thus

$$[Y^0] = \begin{matrix} \frac{R_{22}}{\Delta_0} & -\frac{R_{12}}{\Delta_0} & \frac{R_{12}-R_{22}}{\Delta_0} \\ R_{21} & R_{11} & R_{21}-R_{11} \\ \frac{R_{21}-R_{22}}{\Delta_0} & \frac{R_{12}-R_{11}}{\Delta_0} & \frac{R_{11}+R_{22}-(R_{12}+R_{21})}{\Delta_0} \end{matrix} \tag{15}$$

From (15), the working equations for the different modes of operation are readily obtained by striking out certain rows and columns as shown below.

Grounded base operation: When the base is grounded, the third row and the third column are struck out and we have,

$$[Y_b] = \begin{bmatrix} -\frac{R_{22}}{\Delta_0} & -\frac{R_{12}}{\Delta_0} \\ -\frac{R_{21}}{\Delta_0} & \frac{R_{11}}{\Delta_0} \end{bmatrix}$$

where the subscript b refers to the grounded base mode of operation. The input impedance Z_{in_b} is then given by (Giacoletto, 1953), taking R_L the load resistance into consideration,

$$Z_{in_b} = \frac{R_L(r_{11}\Delta' + r'_{11}\Delta) + \Delta\Delta'}{r_{22}\Delta' + r'_{22}\Delta + R_L\{(r_{11}+r'_{11})(r_{22}+r'_{22}) - (r_{12}+r'_{12})(r_{21}+r'_{21})\}}$$

Similarly, output impedance

$$Z_{out_b} \quad \frac{\Delta\Delta'}{r_{11}\Delta' + r'_{11}\Delta}$$

and forward power gain

$$\phi_b = Z_{in_b} \cdot R_L \cdot \left[\frac{r_{21}\Delta' + r'_{21}\Delta}{\Delta\Delta' + R_L(r_{11}\Delta' + r'_{11}\Delta)}\right]^2$$

It will be noticed that these results are identical with those given by equations (3), (4) and (5).

Grounded emitter operation : When the emitter is grounded, the first row and the first column of the matrix $[Y^0]$ are struck out and then interchanging rows and columns, so that the new arrangement fits in with the grounded emitter circuit, we have,

$$[Y_e] = \begin{bmatrix} R_{11}+R_{22}-(R_{12}+R_{21}) & R_{12}-R_{11} \\ \frac{R_{21}-R_{11}}{\Delta_0} & \frac{R_{11}}{\Delta_0} \end{bmatrix}$$

where the subscript e refers to the grounded emitter mode of operation. Hence, input impedance

$$Z_{in_e} \quad \frac{R_L(r_{11}\Delta' + r'_{11}\Delta) + \Delta\Delta'}{(r_{11}+r_{22}-r_{12}-r_{21})\Delta' + (r'_{11}+r'_{22}-r'_{12}-r'_{21})\Delta + P.R_L}$$

output impedance

$$Z_{out_p} = \frac{\Delta\Delta'}{r_{11}\Delta' + r'_{11}\Delta}$$

and forward power gain

$$\phi_e = Z_{in_p} \cdot R_L \cdot \left[\frac{(r_{21} - r_{11})\Delta' + (r'_{21} - r'_{11})\Delta}{(r_{11}\Delta' + r_{11}'\Delta)R_L + \Delta\Delta'} \right]^2$$

Grounded collector operation: When the collector is grounded, the second row and column of $[Y^0]$ are struck out and interchange of rows and columns are made. This gives input impedance

$$Z_{in_c} = \frac{R_L(r_{22}\Delta' + r'_{22}\Delta) + \Delta\Delta'}{(r_{11} + r_{22} - r_{12} - r_{21})\Delta' + (r'_{11} + r'_{22} - r'_{12} - r'_{21})\Delta + P.\ R_L}$$

output impedance

$$Z_{out_c} = \frac{\Delta\Delta'}{r_{22}\Delta' + r'_{22}\Delta}$$

and forward power gain

$$\phi_c = Z_{in_c} \cdot R_L \cdot \left[\frac{(r_{12} - r_{22})\Delta' + (r'_{12} - r'_{22})\Delta}{(r_{22}\Delta' + r'_{22}\Delta)R_L + \Delta\Delta'} \right]$$

where the subscript c refers to the grounded collector mode of operation.

4. EXPERIMENTAL OBSERVATIONS

Expressions for equivalent parameters, as derived in section 3, were verified by experimental observations under static conditions. Transistors used for this purpose were the following :

Point contact: Philips OC 50 and OC 51.

Junction: Philips OC 70 and OC 71.

For point contact devices, the two transistors were first connected in parallel in the grounded base mode. Biases were then applied and the following observations made :

(i) Variation of collector voltage and emitter voltage with collector current, keeping emitter currents i_e and i'_e constant.

(ii) Variation of collector voltage and emitter voltage with emitter current, keeping collector currents i_c and i'_c constant.

Slopes of the curves obtained from observations (i) and (ii) gave R_{22} and R_{12}, and R_{21} and R_{11} respectively. These R-values and equation (2*b*) were then utilised to compute the elements of the equivalent T-configuration of the parallel combination. Results thus obtained are recorded in row 3, Table I.

The two transistors were then isolated and observations (i) and (ii) repeated on each one of them separately, keeping the values of the parameters (i_e, i'_e, i_c and i'_c) the same as those recorded when observations were made with the two transistors in parallel. These data and equation (2*b*) gave the values of the elements of the equivalent T-configurations of the individual transistors. Results thus obtained are recorded in rows 1 and 2, Table I. Theoretical R-values for the parallel configuration were then computed from these results with the help of equation (13). The computed values are given in row 4, Table I. These are found to be in close agreement with the experimental values obtained earlier.

TABLE I

Point contact transistors

Operating conditions : OC 50 : $i_e = 1.5\ \mu a$; $i_c = -6\ \mu a$.
: OC 51 : $i'_e = 0.6\ \mu a$; $i'_c = -2.3\ \mu a$.

Transistor under observation	r_e Ω	r_b Ω	r_c Ω	r_m Ω
1. OC 50	62	97	3.5 K	10.4 K
2. OC 51	90	147	5.5 K	15.3 K
3. OC 50 & OC 51 (experimental)	56.9	35.4	1.9 K	6.0 K
4. OC 50 & OC 51 (theoretical)	56.8	35	2.1 K	6.0 K

For junction transistors, the type of measurement described above gives rise to some difficulties. For these, measurement of the so called hybrid parameters defined by the following 4-pole equations is more convenient:

$$e_1 = h_{11}i_e + h_{12}e_2$$
$$i_c = h_{21}i_e + h_{22}e_2$$

where h_{11} is an impedance, h_{22} an admittance and h_{12} & h_{21} are ratios.

Note : As in the case of point contact transistors, primed symbols, viz. h'_{11}, h_{12}', h_{21}' etc. will be used here to denote the hybrid parameters of the other junction transistor and capital H letter symbols will be used to denote the hybrid parameters of the combination of the two transistors in parallel.

Unlike the case of the point contact transistors, the two junction transistors were connected in parallel in the grounded emitter mode which was the usual mode of operation for such transistors and base currents i_b and i'_b flowing through the individual transistors at a particular collector voltage V_{cj} say, were noted. The following observations were thereupon made :

(i) variation of collector current and base voltage with collector voltage keeping base currents i_b and i'_b constant,

(ii) variation of collector current and base voltage with base current, keeping collector voltage V_{cj} constant.

H_{22} and H_{12} were determined from observations (i) and H_{21} and H_{11} from observations (ii) by obtaining the slopes of the respective curves. These results were then utilised for obtaining the constants of the equivalent T-configuration for the parallel combination of the two transistors in the grounded base mode of operation by means of the following conversion formulae :

$$\left.\begin{aligned} R_e &= \frac{H_{12}}{H_{22}}; & R_b &= H_{11} - \frac{H_{12}}{H_{22}}(1+H_{21}) \\ R_c &= \frac{1}{H_{22}}(1+H_{21}); & R_m &= \frac{1}{H_{22}}(H_{12}+H_{21}) \end{aligned}\right\} \quad \ldots (16)$$

Results thus obtained are recorded in row 3, Table II.

Tests similar to those enumerated in (i) and (ii) above were thereafter made on the individual transistors with collector voltage maintained at V_{cj} and base currents equal to i_b and i'_b respectively. These tests yielded h_{11}, h_{12}, h'_{11}, h'_{12}, etc. from which the elements of the T-equivalent circuit of the individual junction transistors were determined with the aid of expressions (16). These are given in rows 1 and 2, Table II. Theoretical R values for the parallel combination were then computed with the help of expression (13) and are recorded in row 4, Table II. Results are again found to agree fairly well with those obtained experimentally.

TABLE II

p-n-p Junction transistors

Operating Conditions : OC 70 : $V_{cj} = -2$ volts, $i_b = -10\mu a$
: OC 71 : $V_{cj} = -2$ volts, $i'_b = -15\mu a$

Transistor under measurement	r_e Ω	r_b Ω	r_c Ω	r_m Ω
1. OC 70	50	450	2.05 M	2 M
2. OC 71	28.5	574	1.03 M	1 M
3. OC 70 & 71 (experimental)	17	289	.63 M	.61 M
4. OC 70 & 71 (theoretical)	18	286	.70 M	.67 M

5. CONCLUSION

The problem of two transistors connected in parallel may be analysed by ordinary method of circuit analysis. The analysis of the combination may be

further simplified by reducing it to a single equivalent transistor. The relations between the parameters of this hypothetical transistor and those of the two actual transistors appear in simple form and may be utilised for obtaining readily the expressions for input impedance, output impedance and power gain of parallel transistor amplifier working in any of the three basic modes viz. grounded base grounded emitter and grounded collector configuration. The analysis carried out is found to be essentially correct from the close agreement between some of the crucial theoretical results and those obtained from static experiments with both point contact and junction transistors.

Dynamic characteristics of the parallel combination under actual working condition are under investigation.

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